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EXAMINER	
JOO, JOSHUA	

ART UNIT	PAPER NUMBER
2154	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,688	GEORGIOU ET AL.	
	Examiner	Art Unit	
	Joshua Joo	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-17, 19-20 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, US Patent #6,393,026 in view of Hartmann et al, US Patent #6,047,002 and Nikhil et al, US Patent #5,353,418 (Nikhil hereinafter).

4. As per claim 1, Irwin teaches substantially the invention as claimed including the method and apparatus for a multiprocessing system for connecting two different networks. Irwin's teachings comprise of:

a plurality of programmable processors, each processor having multiple thread units, each thread unit capable of fully executing programs (Col 7, lines 15-20, 40-62. System comprises of programmable computing nodes for executing multiple threads in parallel processing. Col 6, lines 17-26. Individual computing nodes can execute any given procedure.), wherein the thread units are operable for performing communications protocol functions (Col 5, lines 50-22. Packet forward procedures.) using parallel processing (Col 7, line 11); and

a hardware logic front end connected to a network interface for receiving and transmitting data (Col 7, lines 56-61. I/O node of the Central Control Unit (CCU) receives and transmits data packets from networks.), said hardware logic performing time critical operations

(Col 8, lines 8-11; Col 11, lines 9-13. Program counter is initialized for the received data packet.) and communicating received data to and data to be transmitted from said plurality of programmable processors. (Col 9, lines 33-46. The I/O node also communicates received data to and data to be transmitted from the computing nodes.).

5. Irwin teaches the router may connect two different networks (Col 1, lines 16-20). However, Irwin does not specifically teach of performing communications protocol conversion of data frames, and wherein the processors perform the protocol conversion.

6. Hartmann teaches of multiprocessing system, where each processor converts between different types of protocols (Col 2, lines 38-42, 65-68).

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Hartmann because both teachings deal with multiprocessing system that routes packets. Irwin teaches of connecting two different networks, so it would be desirable to convert the protocol of packets traveling between the two different networks. Furthermore, the teachings of Hartmann to convert protocols would enhance the system of Irwin by allowing the router to interface between communication systems employing different packet formats.

8. Irwin does not specifically teach of each processor having multiple thread units, each thread unit capable of fully executing programs and using parallel and pipeline processing.

9. Nikihil teaches of multiprocessor system, where each processor is capable of processing a plurality of threads independently (Col 3, lines 21-24), and where processing is performed in parallel (Col 2, line 68) and pipeline processing (Col 4, line 18)..

10. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Irwin and Nikhil because both teachings deal with multithreaded parallel processing. The teachings of Nikhil for each processor to process multiple threads would improve the efficiency of Irwin's system by increasing the amount of data that is processed. The teachings of Nikhil to provide parallel and pipeline processing would improve the efficiency of Irwin's router because pipeline processing allows the next instructions to be fetched while the processor is performing operations. The result is an increase in the number of instructions that can be performed.

11. As per claim 2, Irwin teaches the system recited in claim 1, wherein each of said programmable processors includes on-chip embedded memory for storing status and control information of current network traffic and for storing received data and data to be transmitted (Col 5, lines 50-67; Col 7, lines 56-63; Col 8, lines 14-17; Col 10, lines 1-19. Each computing node has memory and buffer to queue received information. The computing nodes store received data packets and transmits the data for processing. The computing nodes have packet forwarding programs loaded in the memory used for procedures such as congestion control and performance monitoring.).

12. As per claim 3, Irwin teaches the system recited in claim 2, said embedded memory contains an area dedicated for packet storage, an area where the payload and headers of frames are stored, an area for storing control and status blocks, an area where various protocol specific information and the current status of the network traffic is stored, and an area for working queues, as well as any other information required (Col 5, lines 50-67; Col 7, lines 56-63; Col 8, lines 1-17, 37-60; Col 10, lines 5-7. The computing nodes have memory, and FIFO

buffer for queuing received information. The computing nodes have protocol specific information and procedures for translation, scheduling, and classification, which includes header parameters. The computing nodes store received data packets and have packet forwarding programs used for procedure such as congestion control and performance monitoring.).

13. As per claim 4, Irwin teaches the system recited in claim 3, wherein a beginning address of an inbound data block (IBDB) is added to the master input queue by an input processing unit which manages an IBDB memory area, a "master" thread stored in the master input queue assigning incoming frames to one of a fixed number of threads performing a network protocol, frame dispatching being performed by a workload allocation function which may include workload balancing functionality (Col 6, lines 56-61; Col 7, lines 56-67; Col 10, lines 5-16. As each packet arrives through the I/O node, the master node stores the packet in a buffer and assigns a counter to the program packet. The program packet defines a thread such that that a node executes a queue of procedural calls. The master node performs workload allocation, which includes workload balancing. The master node may limit the number of threads created in a system.).

14. As per claim 5, Irwin teaches the system recited in claim 2,wherein said programmable processors include an on-chip connecting the embedded memory and said multiple thread units (Fig. 7; Col 6, lines 5-16; Col 7, lines 56-61; Col 12, lines 26-27. Processor has multithread hardware connected to memory.).

15. Irwin does not specifically teach of each programmable processor having multiple thread units.

16. Nikihil teaches of multiprocessor system, where each processor is capable of processing a plurality of threads independent (Col 3, lines 21-24.

17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Irwin and Nikhil because both teachings deal with multithreaded parallel processing. The teachings of Nikhil for each processor to process multiple threads would improve the efficiency of Irwin's system by increasing the amount of data that is processed.

18. As per claim 6, Irwin teaches the system recited in claim 5, wherein each of said multiple thread units comprises a register file, a program counter, an arithmetic logic unit, and logic for instruction fetching, decoding, and dispatching (Col 5, lines 50-55, 59-67; Col 6, lines 3-16; Col 11, lines 6-8, 49-64. Thread unit comprises of a register file, counter, and logic for fetching, decoding, and dispatching. An ALU is inherent since the processor executes algorithms.).

19. As per claim 7, Irwin teaches the system recited in claim 5, wherein on-chip high-speed interconnect is implemented as a ring (Col 7, line 45. Interconnect is implemented as a ring.).

20. As per claim 8, Irwin teaches the system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as dual counter rotating rings (Col 7, lines 47-48; Col 9, lines 51-52. Interconnect is a dual ring to provide bidirectional communication to provide the shortest path between nodes).

21. As per claim 9, Irwin teaches the system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as a local bus (Col 8, lines 31-35. Bus).

22. As per claim 10, Irwin teaches the system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as a switch (Col 12, lines 20-22. Switch).

23. As per claim 11, Irwin teaches the system recited in claim 5, further comprising an interprocessor high-speed interconnect connecting said plurality of programmable processors and said hardwired logic front end, and an interconnect interface connecting the on-chip high-speed interconnect of each programmable processor to the interprocessor high-speed interconnect (Col 7, lines 44-45; Col 8, lines 28-36; Col 12, lines 30-31. High-speed interconnect connects the plurality of processors and the I/O node. The nodes have a transmission interface connected to the ring.).

24. As per claim 12, Irwin teaches the system recited in claim 11, wherein said hardwired logic front end comprises:

A receiver and a transmitter connect to port logic, said receiver outputting received frame data and said transmitter receiving frame data to be transmitted (Fig, 10, #174. Receive FIFO and Transmits FIFO);

An inbound interface which receives frame data output by said port logic (Fig. 10, #174 "Transmitter"); and

An outbound interface which outputs frame data to be transmitted to said port logic, said inbound interface and said outbound interface being connected to said interprocessor high-speed interconnect (Fig.10, #174. "Receiver" I/O interface receives data and transmits data packets. I/O interface has am inbound interface which receives frame data and a outbound interface which receives packets for output.).

25. Irwin does not teach of

A second receiver and a second transmitter connected to second port logic, said second receiver outputting received frame data according to a second protocol and said second transmitter receiving frame data according to the second protocol;

A second inbound interface which receives frame data output by said second port logic; and

A second outbound interface which outputs frame data to be transmitted to said second port logic, said second inbound interface and said second outbound interface being connected to said interprocessor high-speed interconnect.

26. Hartmann teaches of plurality of a plurality of inputs and outputs for receiving packet and transmitting packet data (Abstract). Each port adaptor comprises of a communication port for receiving and transmitting data, where a FIFO buffer is coupled to each port adaptor (Col 5, lines 5-10). Each port adaptor is configured to receive different types of communication packet formats (Col 2, lines 37-43).

27. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Hartmann because both teachings deal with forwarding of packets across different networks. Furthermore, the teachings of Hartmann to have multiple transmitters and receivers to receive and transmit packets from different networks that use different protocols and to transmit packets to the buffer would enhance the router of Irwin by allowing the router to process and forward more packets from various different networks.

28. As per claim 20, Irwin teaches of system with a plurality of processors for connecting two different networks (Col 1, lines 17-20; Col 5, lines 35-36). However, Irwin does not specifically the teach the system recited in claim 1, wherein the system converts between two protocols, and the system comprises four processors, and wherein:
a first processor provides inbound processing for a first protocol;
a second processor provides outbound processing for the first protocol;
a third processor provides inbound processing for a second protocol; and
a fourth processor provides outbound processing for the second protocol.

29. Hartman teaches of providing a multiprocessor system, where each protocol processor is operable to convert between one or more communication formats (Col 2, lines 37-42).

30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Hartmann because both teachings deal with multiprocessing systems capable of connecting different networks. Furthermore, it would have been obvious for each processor to perform protocol conversion and be assigned a specific function because doing so would improve the efficiency of Irwin's system by utilizing all the processors and allowing the router to interface between different communication systems.

31. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, Hartmann, Nikhil in view of Hartwell, US Patent #6,629,257.

32. As per claim 13, Irwin does not teach the system recited in claim 12, further comprising a phase locked loop supplying clock signals to said receiver and said transmitter.

33. Hartwell teaches of a phase locked loop supplying clock signals to an input/output (I/O) subsystem (Col 2, lines 29-33).

34. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Hartwell because the teachings of Hartwell to use phase locked loop to supply clock signals to the I/O subsystem improves the invention of Irwin by stabilizing communications by keeping it set to a particular frequency.

35. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, Hartmann, Nikhil in view of Dwork et al, US Patent #5,513,354 (Dwork hereinafter).

36. As per claim 14, Irwin teaches of monitoring the activity of hardware resources and allocating the work to least loaded processors (Col 6, lines 56-61).

37. Irwin does not teach of re-allocating workload to resources that are not heavily utilized.

38. Dwork teaches an invention for managing tasks in a multiprocessing system, where workload is reallocated to processors, where the workload is balanced among the processors (Col 5, lines 53-56; Col 6, lines 35-38; Col 8, lines 5-9).

39. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Dwork because both inventions deal with a multiprocessing system in a ring network. Irwin's teaches of providing high processing utilization, so reallocating work from a processor would be a desirable feature in the system of Irwin. Furthermore, the teachings of Dwork to reallocate workload to resources that are not heavily utilized would improve the efficiency of Irwin's teachings by increasing the utilization of the processing resources.

40. As per claim 15, Irwin, Hartmann, Nikhil, and Dwork taught the system recited in claim 14. Irwin further teaches wherein the built-in monitors examine work queues of said programmable processors (Col 6, line 62-Col 7, line 2. Monitors queues of the processors.).

41. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, Hartmann, Nikhil, Dwork in view of Iwashita et al, US Patent #4,674,034 (Iwashita hereinafter).

42. As per claim 16, Irwin does not specifically teach the system recited in claim 14, wherein the built-in monitors examine memory resources of said programmable processors.

43. Iwashita teaches of a multiprocessor system that provides high-speed processing, where the amount of data stored in the memory is monitored and data input is stopped when the data amount exceeds capacity (Col 16, lines 46-50).

44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Iwashita because both teachings deal with allocating work in a multiprocessing system. Irwin teaches of checking the queue level of the processors to allocate work in order to provide high utilization of the processors, thus it would be desirable to monitor the memory resources as well. The teaching of Iwashita to monitor the memory resources would improve the utilization of the system of Irwin by preventing an overflow in the queue memory.

45. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, Hartmann, Nikhil, Dwork in view of Seaman, US Patent #5,428,766.

46. As per claim 17, Irwin does not teach the system recited in claim 14, wherein the built-in monitors examine interconnection resources of said plurality of programmable processors.

47. Seaman teaches an invention for a multiprocessor system where a monitor examines the bus activity of communications of messages through the buffer memory and the ring memory (Col 9, lines 36-41).

48. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Seaman because both teachings deal with multiprocessor systems. The teaching of Seaman to examine the interconnection resources would improve the teachings of Irwin by allowing for regulation of the traffic flow, preventing an inflow of data to a processor.

49. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, Hartmann, Nikhill, and in view of Gamo, US Publication #2001/0025324.

50. As per claim 19, Irwin and Nikhil does not teach the system recited in claim 1, wherein the protocol conversion of data frames is performed such that related data frames are dispatched to the same thread unit.

51. Reeve teaches of executing objects that have execution seriality in the same thread (Paragraph 0039).

52. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin, Nikhil, and Reeve because the teachings of Reeve to process related objects in the same thread would improve the parallel processing system of

Irwin and Nikhil by increasing the efficiency of processing data by reducing traffic within the system.

Response to Arguments

53. Applicant's arguments filed 5/16/2005 have been fully considered but they are not persuasive.

54. Applicant argues (1) Irwin does not teach or suggest communications protocol conversion, as required by amended claim 1; (2) In the present invention, there is no master processor and no slave processors; (3) Adiletta completely lack any teaching or suggestion of protocol conversion; (4) Neither Irwin nor Adiletta teach memories with areas for storage of payload and header information, or storage areas for protocol-specific information; and (5) Neither Irwin nor Adiletta et al. teach or suggest separately storing header and payload data information.

Examiner traverses the argument:

55. As to point (1), Irwin teaches of a router for processing data packets, where the IP router may be used to forward packets between different networks (Col 1, lines 16-19). In forwarding packets between two different networks, it would have been obvious to include the process of converting protocols. Mergard, US Patent #5,881,248, teaches of routing messages across different networks, where the routing involves translating between different protocols (Col 3, lines 41-46). Finn et al, US Patent #5,826,032, teaches of an IP layer gateway, also known as an IP router, that connects two different networks by converting between different network topologies (Col 4, lines 54-63). Murthy et al, US Patent #5,610,905, also teaches of a bridge or

router that forwards packets between different networks (Col 1, lines 20-24), where the forwarding involves translating packets from one protocol format to another (Col 22, lines 25-28). Hartmann also teaches of an apparatus for interfacing between communication systems employing different packets, where interfacing involves converting between different types of communications packet (Col 2, lines 7-9, 38-42). Thus, Irwin's teachings of forwarding between two different network suggests of converting protocols, and it would have been obvious to combine Irwin and Hartmann to specifically teach that forwarding packets between two different networks would involve protocol conversion.

56. As to point (2), claim 1 does not specifically state that there is no master processor and slave processors. Claim 1 discloses a plurality of programmable processors, where Irwin also teaches of a multiprocessor system (Col 5, lines 40-43). It is noted that the features upon which applicant relies (i.e., Lack of master/slave processing system) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

57. As to point (3), Adiletta has been withdrawn from the rejection due to applicant's amendments. However, claim 1 is now rejected Irwin in view of Hartmann and Nikhil, where Hartmann teaches of protocol conversion.

58. As to point (4), Irwin teaches of storing information regarding the header, where Irwin teaches that the processor contains information regarding the translation of the header (Col 5, lines 50-53). Information regarding the translation of the header would indicate that the router is

storing header information. Also, in the applicant's specification, paragraph 0026, applicant defines payload as payload of the frame (i.e. data), where storing is performed in the FIFO. Irwin teaches of storing the data packet in a packet buffer (Col 10, lines 5-6), thus Irwin teaches of storing payload information. As to applicant's argument that Irwin does not teach of storing protocol-specific information, Irwin teaches of having information for the translation of the header, classification of the packet, and service routing. This information is regarding to the currently used protocol in the invention, such as IP (Col 1, lines 14-15). Therefore, Irwin's teachings would indicate that the router stores protocol information in order to route packets.

59. As to point (5), in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., separate storage of header and payload data information) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

60. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

61. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

> Burns et al, US Patent #6,895,013, teaches of multiprocessor system, where processing involves parallel and pipeline processing.

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Joo whose telephone number is 571 272-3966. The examiner can normally be reached on Monday to Friday 7 to 4.

63. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A. Follansbee can be reached on 571 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

64. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 30, 2005
JJ